TÜBİTAK

UME

17RPT03 DIG-AC

WP1: Digitizer Evaluation

19/05/2022

Madrid, Spain

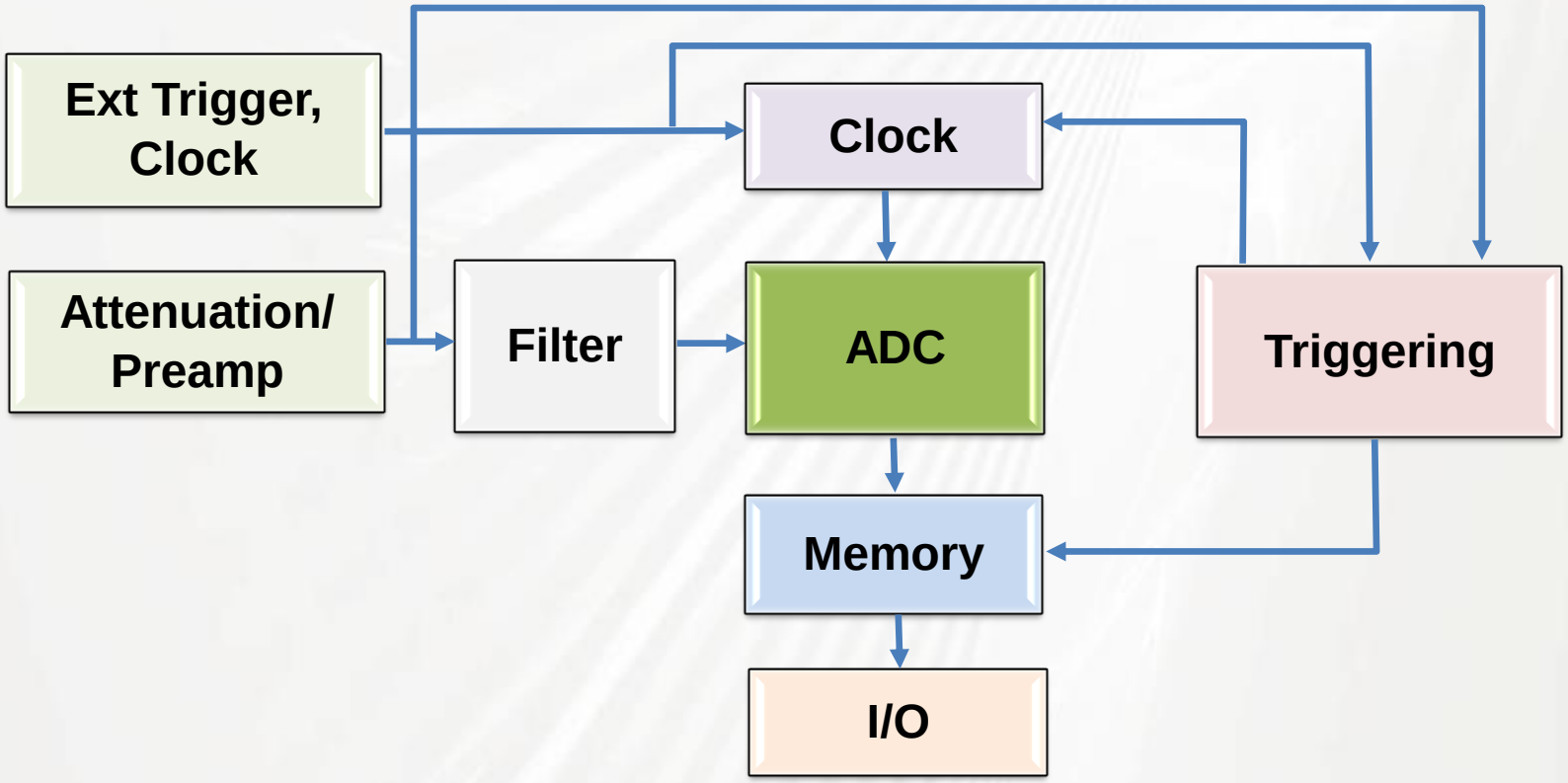
WP1, Objectives

- The aim of this work package was to select and plan the testing of digitizers used to link digital electrical measurements to recently developed quantum voltage standards.

- WP included tasks of:
  - ✓ Research that will determine the needs of stakeholders and the market (Task 1.1),
  - ✓ The selection of 3 common digitizers meeting the necessary conditions (Task 1.2)
  - ✓ Preparation of the plan for validation of the selected digitizers (Task 1.3).

Digitizer

Electronic acquisition device that acquire analogue waveforms, process them through ADCs and send the digitized sample to a buffer, which allows them to be saved before being processed by a computer.



Task 1.1 Requirements for Digitizer Selection

Determine the needs of stakeholders and the market.

Stakeholders:

- NMIs
- Primary & Secondary laboratories
- Measurement Devices Manufacturers
- Academic Institutions

Needs:

- AC Voltage
- AC Current
- Electrical Power
- Impedance
- Various quantities based on dynamic sensor measurements (force, pressure, temperature, vibrations, etc)

Task 1.2 Digitizer Selection

AC Voltage, basic requirements:

✓ Range: 100 mV – 1 Vrms @ DC – 1 MHz

✓ Uncertainty: ≤ 25 µV/V @ 1 V, 1 kHz

- Voltage traceability up to 1000V:

Combining with the wideband voltage dividers developed in the scope of the other projects e.g. QuADC

- Voltage traceability down to 1 mV:

Combining with the special designed amplifiers

- Current

Combining with the special designed current shunts

Task 1.2 Digitizer Selection…

Parameters used to specify the digitizer:

Parameter	Value
Input Range	1 Vrms
Input Impedance	≥1 MΩ
Resolution	≥20 Bits
Bandwidth	5 MHz
Sample Rate	15 MS/s
Accuracy (Uncertainity)	0,0025 %
Trigger/Clock	Ext Trigger, Ext Clock
Internal Memory	≥1 MB
CMRR	≥100 dB
Software	LabView, LabWindows …

Task 1.2 Digitizer Selection…

Model	Input Range	Input Impedance	Resolution	Bandwidth	Sample Rate	Triger/Clock	Internal Memory	Software	Other
Adlink PXI-9527	Selectable: ±(0.3–40) V	50Ω/1MΩ	24 Bit	130 kHz	432 kS/s (24Bit)	Ext Triger PXI Clock	2048 S	LabView	PXI, 2 ch
Applicos WFD22	Selectable: ±(0.4–10) V	1MΩ	22 Bit	1 MHz	1 MS/s	Ext Triger Ext Clock	32 MS	LabView	ATX
Applicos WFD20	Selectable: ±(0.5–8) V	1MΩ	20 Bit	2 MHz	2 MS/s	Ext Triger Ext Clock	4 MS	LabView	ATX
Applicos WFD16	Selectable: ±(0.5–8) V	50Ω/1MΩ	16 Bit	100 MHz	180 MS/s	Ext Triger Ext Clock	8 MS	LabView	ATX
Astronix PXIe-1803	Selectable: ±(0.5–30) V	50Ω/1MΩ	16 Bit	175 MHz	180 MS/s	Ext Triger Ext Clock	64 MS	LabView	PXIe, 2 ch
Keithley DMM7510	Selectable: ±(0.1–1000) V	10GΩ/10MΩ	18 Bit	600 kHz	1 MS/s	Ext Triger Ext Clock	8 MS	LabView	Standalone
Keysigth 3458A	Selectable: ±(0.1–1000) V	10GΩ	28 Bit	150 kHz	1 MS/s	Ext Triger Ext Clock(m)	48 kS	LabView	Standalone
Nat.Instruments 5922	Selectable: ±(2, 10) V	50Ω/1MΩ	24 Bit	6 MHz	15 MS/s	Ext Triger Ext Clock	64 MS/ch	LabView	PXI, 2 ch
Nat.Instruments 9225	300 V	1MΩ	24 Bit	25 kHz	50 kS/s	--	--	LabView	NI CompactRio
Spectrum MX.4963	Selectable: ±(0.2 – 10) V	50Ω/1MΩ	16 Bit	30 MHz	50 MS/s	Ext Triger Ext Clock	64 MS/ch	LabView	Standalone, 4 ch
Tasler LTT24	Selectable: ±(0.3 – 50) V	50Ω/1MΩ	24 Bit	1.7 MHz	4 MS/s	Ext Triger Ext Clock	32 MS/ch	LabView	Standalone, 4 ch
VXInstruments PXD€721x	Selectable: ±(0.25–60) V	50Ω/1MΩ	16 Bit	100 MHz	100 MS/s	Ext Triger PXI Clock	2 MS	LabView	PXIe, 2 ch
Zurich Instr. MF-DIG	Selectable: ±(0.001–3) V	50Ω/1MΩ	24 Bit	7 MHz	60 MS/s	Ext Triger Ext Clock	2.5 MS/ch	LabView	Standalone 2 ch

Task 1.2 Digitizer Selection…

- National Instruments 5922, Tasler LTT24, Applicos WFD20/22, Zurich Inst. MF-DIG

Best resolution – bandwidth performances

- Astronix PXIe-1803, Applicos WFD16, VXInstruments PXD€721x, Spectrum MX.4963

Fair resolution and large bandwidth

- Keysigth 3458A, Fluke 8X58A, Keithley 7510

Ideal for low frequency applications

<u>D1: Report on the selection of three digitisers and their parameters that meet the necessary requirements for digital traceability chain</u>

Task 1.3 Plan for verification of the digitizers

List of the Test Parameters of Digitizers:

Specification	Test Parameter
Input Range	• Static Offset • Static Gain • Static Gain Drift (Temperature) • Integral non-linearity (INL) • Differential non-linearity (DNL) • Static Gain Stability
Input Impedance	• Input Impedance
Dynamic Range	• Signal-to-noise ratio with distortion/ Effective number of bits SINAD/ENOB • Total Harmonic Distortion (THD) • Spurious Free Dynamic Range (SFDR)
Frequency Response	• Bandwidth • Dynamic gain, Flatness • Dynamic gain, Level dependence • Dynamic gain, Stability • CMRR • Crosstalk (for 2-ch digitizers):
Synchronization/Trigger	• Phase (for 2-ch digitizers)

Task 1.3 Plan for verification of the digitizers

Specification	Parameter	Test Method
Input Range	Static Offset	[1], 6.1, pg 83 [2], 7.4.1 pg 44
	Static Gain	[1], 6.1, pg 83 [2], 7.4.1 pg 44
	Static Gain Drift (Temperature)	Perform static gain test at different environmental temperatures
	Integral non-linearity (INL)	[1], 7.1.2, pg 85 [2], 8.2.1 pg 46
	Differential non-linearity (DNL)	[1], 7.3.2, pg 86 [2], 8.4.1 pg 47
	Static Gain Stability	Repeat static gain test during a specific period
Impedance	Input Impedance	[1], Chapter 5.1, pg 81 [2], Chapter 7.2.1 pg 44
Dynamic Range	SINAD/ENOB	[1], Chapter 8.1, pg 105 [2], Chapter 9.2, pg 65
	Total Harmonic Distortion (THD)	[1], Chapter 7.7, pg 91 [2], Chapter 8.8, pg 51
	Spurious Free Dynamic Range (SFDR)	[1], Chapter 8.8, pg 112 [2], Chapter 8.8.2, pg 56
Frequency Response	Bandwidth	[1], Chapter 10.1, pg 127 [2], Chapter 11.1, pg 76
	Dynamic gain, Flatness	[1], Chapter 10.2, pg 127 [2], Chapter 11.2, pg 78
	Dynamic gain, Level dependence	[1], Chapter 10.3, pg 128 [2], Chapter 11.3, pg 78
	Dynamic gain, Stability	Repeat dynamic gain test during a specific period
	CMRR	[1], Chapter 15.2, pg 140 [2], Chapter 14.4.2, pg 96
	Crosstalk (for 2-ch digitizers):	[1], Chapter 11.1, pg 133
Synchronization/Trigger	Phase	

[1] IEEE Standard for Digitizing Waveform Recorders

[2] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

Task 1.3 Plan for verification of the digitizers

Test procedures in current IEEE standards are based on electronic instrumentation.

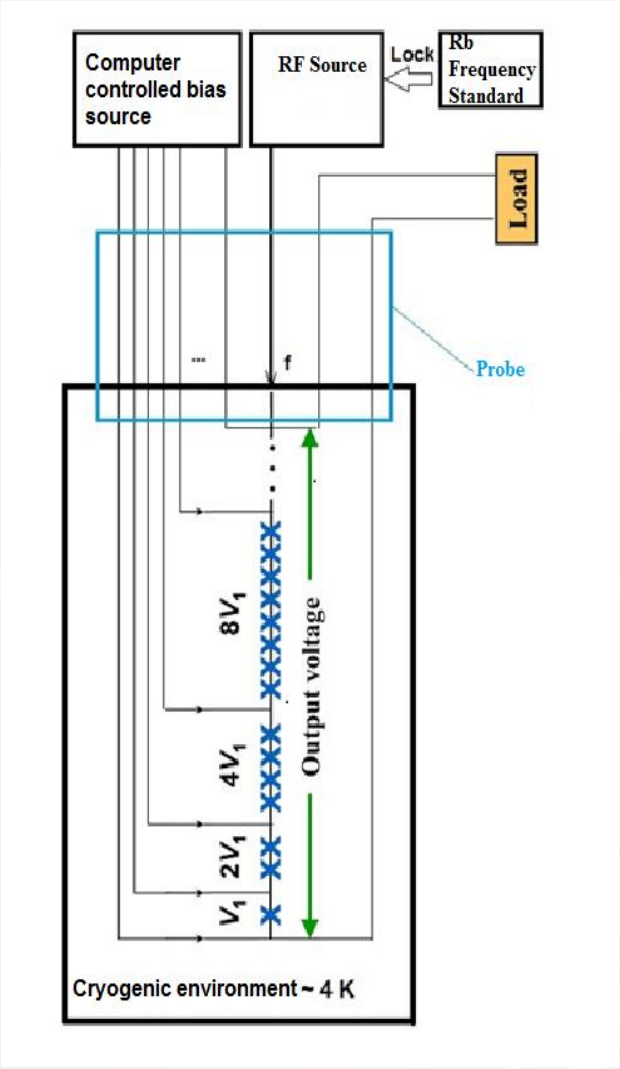
Linearity of a 28-bit digitizer (3458A) is specified below 0.1 ppm, and no any electronic instruments today can provide such accuracy.

Quantum standards:

- ✓Programmable Josephson Voltage Standard (PJVS)
- ✓Josephson Arbitrary Waveform Synthesizer (JAWS)

Task 1.3 Plan for verification of the digitizers

Programmable Josephson Voltage Standard (PJVS)

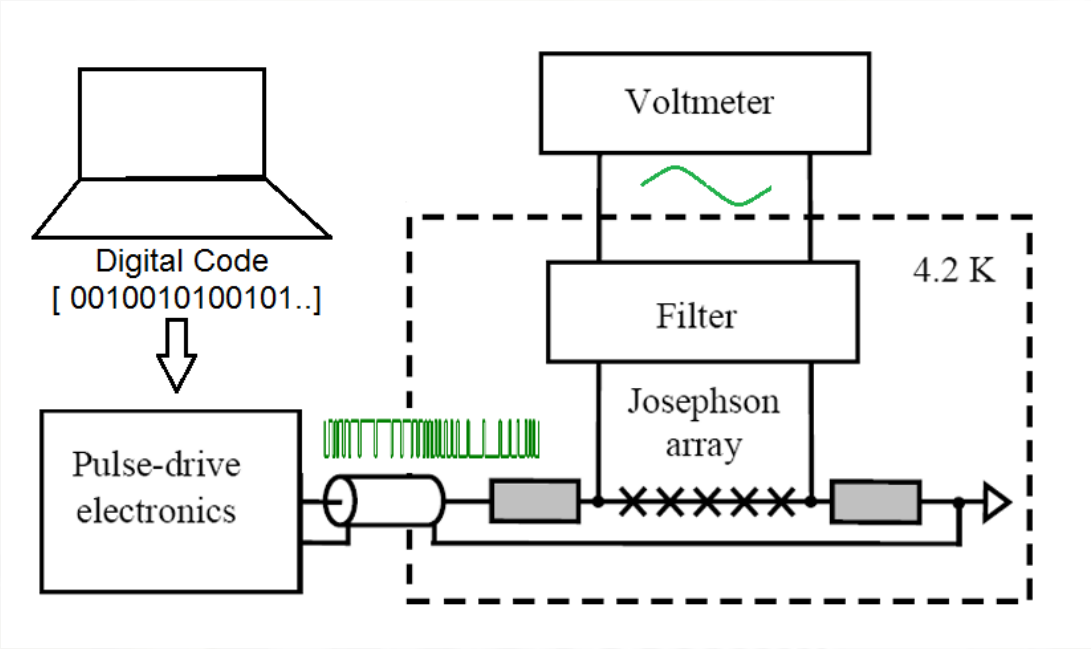


Parameter	Programmable Josephson Voltage Standard (PJVS)
Voltage Range	±10 V, 7 V rms
Frequency	DC to 100 kHz*
Accuracy	DC: ±10 V, $\Delta V/V_{10V} = 1\times10^{-10}$ AC: $\Delta V/V = 5\times10^{-7}$ @ V ≤ 7.1 V rms, ≤ 1 kHz, 1 min meas. time** Limit of calibrator, otherwise 1×10^{-8}
SFDR	-
Synchronization	Yes

* differential sampling up to 10 kHz and sub-sampling up to 100 kHz
** Fluke 5720A ACV calibration

Task 1.3 Plan for verification of the digitizers

Josephson Arbitrary Waveform Synthesizer (JAWS)



Parameter	Josephson Arbitrary Waveform Synthesizer (JAWS)
Voltage Range	1 V rms (PTB), 3 V rms (NIST)
Frequency	DC - 1 MHz
Accuracy	Best; 12 nV/V @ 250 Hz
SFDR	120 dBc
Synchronization	Yes

Task 1.3 Plan for verification of the digitizers

Parameter	PJVS	JAWS
Static Offset	√	√ (2)
Static Gain	√	√ (2)
Static Gain Drift (Temperature)	√	√ (2)
Integral non-linearity (INL)	√	√ (2)
Differential non-linearity (DNL)	√	√ (2)
Static Gain Stability	√	√ (2)
SINAD/ENOB	√ (1)	√
Total Harmonic Distortion (THD)	√ (1)	√
Spurious Free Dynamic Range (SFDR)	√ (1)	√
Bandwidth	√ (1)	√
Dynamic gain, Flatness	√ (1)	√
Dynamic gain, Level dependence	√ (1)	√
Dynamic gain, Stability	√ (1)	√
CMRR	√ (1)	√
Crosstalk (for 2-ch digitizers)	√ (1)	√

Report on the best quantum-based system verification approach for testing digitizers to provide digital traceability chain for AC voltage and current (D2)

Thank you for your attention!

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